APPLICANT'S BRIEF ON APPEAL

On August 10, 2006, all claims were finally rejected by the Examiner. On September 18, 2006, the Applicant filed a Notice of Appeal. Together with this Brief, the Applicant has filed a Petition for a five month extension of time. The extension of time extends the *non-statutory* two months from notice of appeal time period to seven months from notice of appeal, making this brief timely.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest is Transwitch Corporation by virtue of an assignment recorded at Reel: 014483, Frame: 0038.

II. Related Appeals and Interferences

There are no other appeals or interferences which are related to this application or this appeal.

III. Status of the Claims

This application was filed with claims 1-20. There have been no amendments to or cancellations of the claims. All claims stand finally rejected.

IV. Status of Amendments

No amendments were submitted after final rejection.

V. Summary of the Claimed Subject Matter

Independent claim 1 is directed to an integrated circuit chip (10 in Figure 1) which includes core logic (12 in Figure 1), an on-chip JTAG TAP (14 in Figure 1) coupled to the core logic, an on-chip JTAG master (16 in Figure 1) coupled to the JTAG TAP, and an on-chip microprocessor interface (20 in Figure 1) coupled to the JTAG master. This is generally described at page 7, lines 7-16 of the application. It is also described in summary fashion at page 5, lines 11-21 and the advantages of this arrangement are described at page 5 line 23 through page 6, line 13.

Dependent claim 6 recites switching means for selectively decoupling the JTAG interface (introduced in claim 5) from the JTAG TAP. This is generally shown in Figure 2 and generally includes elements 22, 24, 26, and 36. The switching means is also described in part at page 7, line 18 through page 8, line 5. It is further described at page 13, line 17 through page 14.

Independent claim 9 is directed to an integrated circuit chip (10 in Figure 1) which includes core logic (12 in Figure 1), an on-chip JTAG TAP (14 in Figure 1) coupled to the core logic, an on-chip JTAG interface (28, 30, 32, 34, and TDO in Figure 1) selectively coupled to the JTAG TAP, an on-chip microprocessor interface (20 in Figure 1) selectively coupled to the JTAG TAP and switching means for selectively coupling the JTAG interface and microprocessor interface to the JTAG TAP. This is generally described at page 7, lines 7-16 of the application. It is also described in summary fashion at page 5, lines 11-21 and the advantages of this arrangement are

described at page 5 line 23 through page 6, line 13. The switching means is generally shown in Figure 2 and generally includes elements 22, 24, 26, and 36. The switching means is also described in part at page 7, line 18 through page 8, line 5. It is further described at page 13, line 17 through page 14.

Dependent claim 16 recites means for performing TAP operations having bit counts in excess of N-bits (the size of the FIFOs involved). This is described at page 11, line 7 through page 13, line 15 and relies in part on the FIFOs (18 in Figure 1) which are described at page 8, line 7 through page 9, line 1 as well as page 10, line 16 through page 11, line 5, the TAP state machine (14 in Figure 1), and the microprocessor (not shown).

Dependent claim 17 includes means for cycling the TAP through state elements and holding it in one of four states. This is described at page 11, line 7 through page 13, line 15 and relies in part on the FIFOs (18 in Figure 1), the TAP state machine (14 in Figure 1), and the microprocessor (not shown).

Independent claim 19 is directed to an integrated circuit chip (10 in Figure 1) which includes core logic (12 in Figure 1), an on-chip JTAG TAP (14 in Figure 1) coupled to the core logic, an on-chip JTAG master (16 in Figure 1) selectively coupled to the JTAG TAP, an on-chip JTAG interface (28, 30, 32, 34, and TDO in Figure 1) selectively coupled to the JTAG TAP, and switching means for selectively coupling the JTAG interface and JTAG master to the JTAG TAP. This is generally described at page 7, lines 7-16 of the application. It is also described in summary fashion at page 5, lines

11-21 and the advantages of this arrangement are described at page 5 line 23 through page 6, line 13. The switching means is generally shown in Figure 2 and generally includes elements 22, 24, 26, and 36. The switching means is also described in part at page 7, line 18 through page 8, line 5. It is further described at page 13, line 17 through page 14.

VI. Grounds of Rejection to be Reviewed on Appeal

The sole issue on appeal is whether claims 1-20 are unpatentable under 35 U.S.C. §103(a) as obvious over Texas Instruments Document SCBS676D-December 1996-Revised August 2002 (hereinafter "Texas Instruments") in view of Patavalis.

VII. Argument

The Examiner's rejection of independent claims 1, 9, and 19 can be summarized with the following statements taken from the first Office Action: The eTBC (embedded test-bus controller) in Texas Instruments is similar to a JTAG (Joint Test Action Group) master. Patavalis teaches core logic on the same chip as a JTAG TAP (test access port). It would have been obvious to combine the teachings and put the eTBC on the same chip as the core logic and JTAG TAP. According to the Examiner, the incentive for making the combination would have been to "provide the opportunity to access and control the signal-levels on the pins of a digital circuit and test the internal circuitry on the chip." The Examiner did not state where that alleged incentive could be found, but it appears to be taken from the Abstract of the Patavalis paper which is entitled "A Brief Introduction to the JTAG Boundary Scan Interface". The ability to access and control the signal-levels on the pins of a digital circuit and test the internal circuitry on the chip is, according to Patavalis, the general goal of the JTAG boundary scan which is defined by the IEEE 1149.1 standard. In other words, that goal has already been met by IEEE 1149.1 and there is no need to do anything else in order to achieve that goal. The IEEE 1149.1 standard specifies that the JTAG master be implemented on a separate chip from the chip which includes the core logic and the JTAG TAP. Therefore, the Examiner's stated incentive to combine TAP and master on the same chip is actually a disincentive to combine.

Both of the cited documents, which were submitted by the applicant, teach that the JTAG boundary scan is accomplished by providing a JTAG TAP together on the same chip as the integrated circuit (core logic) to be tested, providing a JTAG master

(also referred to in Patavalis as a TAP controller) on another separate chip which is coupled to the first chip via the TAP and providing a microprocessor on a third chip which is coupled to the JTAG master. Memory is provided on yet a fourth chip. See, e.g., Figure 1 on page 5 of Texas Instruments.

The Examiner's first Office Action ignored the fact that the invention claimed is a single integrated circuit chip which contains multiple JTAG components which the prior art locates on separate chips. Throughout the specification it is made clear that the invention is directed to a single chip which contains multiple JTAG components. The preamble of claim 1 is directed to "an integrated circuit chip". All of the JTAG components are described in the claim as "on-chip". It is impossible to interpret claim 1 in any other way.

Following the first Office Action, an attorney for the applicant spoke by telephone with the Examiner and the Examiner agreed that there was no teaching or suggestion to include a JTAG TAP and a JTAG master on the same chip. An Examiner's Interview Summary (paper no. 20060522) confirms this understanding and indicates that agreement with respect to claim 1 was reached. The Interview Summary is signed by both the Examiner and his Supervisor. The Applicant filed its own interview summary and expected that a Notice of Allowance would follow. Instead, a final rejection issued.

The final rejection correctly summarized the Applicant's position that "although the prior art shows all of the elements of claim1, they are not all on the same chip." In

response to this argument the Examiner states that Texas Instruments teaches "to master ... JTAG TAP under the command of an embedded host microprocessor/microcontroller." This doesn't explain anything. The Examiner also pointed out that eTBC is similar to a JTAG master. This still doesn't explain the Examiner's change of opinion regarding claim 1. Finally, the Examiner rejected the remaining claims by stating that "the same arguments apply to independent claims 9 and 19."

A. Claim 1

Claim 1 calls for a JTAG TAP and JTAG master to be on the same chip with the core logic. The prior art does not teach or suggest combining these elements on a single chip. In fact, the prior art specifically teaches placing the JTAG TAP and JTAG master on separate chips. One of the reasons why the master is on a separate chip is that a typical implementation of IEEE1149.1 uses one master to test multiple chips coupled to a bus, hence the term "test-bus controller" used by Texas Instruments. See, e.g., Figure 5 of Texas Instruments. As set forth above, the Examiner's alleged incentive for placing the JTAG TAP and JTAG master on the same chip is not a true incentive as the goals stated in the incentive are accomplished by the prior art without the combination on the same chip. In addition Texas Instruments and Patavalis teach away from combining these two elements on the same chip. In light of the above it is clear that claim 1 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

B. Claim 2

Claim 2 specifies that the chip also contains a plurality of registers coupled to the microprocessor interface and to the JTAG master. As shown in the prior art, these registers are provided on yet another chip separate from the chip containing the JTAG TAP and separate from the chip containing the JTAG master and separate from the chip containing the microprocessor. The fact that the elements in the prior art are on separate chips is ignored by the Examiner. Therefore, claim 2 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

C. Claim 3

Claim 3 specifies what kind of registers (a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register) are included on the chip and these are some of the registers used in performing the JTAG boundary scan. While these registers are known in the art, the art neither teaches nor suggests that they be on the same chip as the TAP and the master and the core logic. Therefore claim 3 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

D. Claim 4

Claim 4 specifies that the registers include a start bit register and an end bit register. The Examiner refers to pages 14 and 15 of Texas Instruments which describe various registers. However, none of the registers is a start bit register or an end bit

register. The combination of art cited by the Examiner therefore fails to even recite all of the claimed limitations. Therefore claim 4 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

E. Claim 5

Claim 5 is most easily understood with reference to Figure 1 of the instant application. Claim 5 specifies that the chip has more than five pins and five of the pins (TRST, TMS, TCK, TDI, and TDO) are coupled to the on-chip JTAG TAP 14 forming a JTAG interface to said chip 10. In rejecting claim 5, the Examiner refers to Figure 1 of Texas Instruments, implying that the components shown are all on a single chip. This is clearly not the case, however. All known prior implementations of the JTAG standard provide the TAP and the master on separate chips. Moreover, the JTAG interface is essentially a TAP for use by an off-chip master. Thus, the chip has two TAPS, one internal to be used by an on-chip master and one defined by the five pins for use with an off-chip master. No chip in the prior art shows two TAPs on the same chip. The combination of art cited by the Examiner fails to even recite all of the claim limitations. Therefore claim 5 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

F. Claim 6

Claim 6 adds the switching means 22, 24, 26, 36 in Figure 2 to claim 5 so that the JTAG interface (TRST, TMS, TCK, TDI, and TDO) can be decoupled from the JTAG TAP 14. In rejecting claim 6, the Examiner refers to page 13 of Texas Instruments which specifies that the host can disable the output of the target, the host being the microprocessor in Figure 1, page 5 and the target being the device under test. The prior art does not teach or suggest placing the switching means on the same chip as the TAP and the master. According to the prior art, an external register and external microprocessor are required to switch off the output of the TAP. Therefore claim 6 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

G. Claim 7

Claim 7 further specifies that the switching means is coupled to and controllable by the JTAG master 16 which, as specified in parent claim 1, is on the same chip. According to the cited portion of Texas Instruments, the switching means is not controlled by the JTAG master but is controlled by the host (microprocessor) and the host, the master, and the TAP are all on separate chips. Therefore claim 7 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

H. Claim 8

Claim 8 specifies that the switching means couples the JTAG master 16 to the JTAG TAP 14 when the JTAG interface (TRST, TMS, TCK, TDI, and TDO) is decoupled from the JTAG TAP, and couples the JTAG interface to the JTAG TAP when the JTAG master is decoupled from the JTAG TAP. The Examiner refers to Texas Instruments Fig. 1, and pages 5, 6, 9, and 13. However, the only teaching in Texas Instruments regarding switching is the toggling of the NTOE bit which toggles the TAP output on and off. This substantially decouples the TAP from the master, but it does not couple the TAP to anything else. Moreover, the switching means described by Texas Instruments is not on a single chip together with the TAP, the master, and the JTAG interface. In addition, Texas Instruments does not disclose or suggest a JTAG interface other than the TAP. As the term is defined in the specification and as can be gleaned from Figure 1 of the application, the JTAG interface is an extension of the on-chip TAP to five pins on the chip. This allows the chip to be used in a conventional manner, i.e. with an off-chip JTAG master, when the switching means couples the JTAG interface to the JTAG TAP. It also allows the chip to be used in the inventive way when the switching means couples the JTAG master 16 to the JTAG TAP 14. Therefore claim 8 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

I. Claims 9 and 12

Independent claim 9 is drawn to an integrated circuit chip having core logic, an on-chip JTAG TAP, an on-chip JTAG interface, an on-chip microprocessor interface, and

switching means for selectively coupling the TAP to either the JTAG interface or the microprocessor interface. As described above with respect to claim 8, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. In addition, the prior art does not show a TAP, a JTAG interface, and a microprocessor interface all on the same chip. The Examiner's alleged incentive for combining JTAG elements on the same chip is not a true incentive as the goals stated in the incentive are already accomplished by the prior art without the combination on the same chip. In addition Texas Instruments and Patavalis teach away from combining these elements on the same chip. Therefore claim 9 and claim 12 which depends therefrom are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

J. Claim 10

Claim 10 further clarifies that the switching means decouples the TAP from the JTAG interface when the TAP is coupled to the microprocessor interface and decouples the TAP from the microprocessor interface when the TAP is coupled to the JTAG interface. As described above, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Therefore claim 10 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

K. Claim 11

Claim 11 further specifies that the microprocessor interface includes a plurality of registers. As shown in the prior art, these registers are provided on yet another chip separate from the chip containing the TAP and the chip containing the microprocessor. There is no suggestion in the prior art to put all of these components on a single chip. Therefore claim 11 is allowable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

L. Claims 13 and 14

Claim 13 further specifies a switching means enable interface which enables or disables the switching means. As described above, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Moreover, there is no switching means enable interface shown in the prior art. Therefore claim 13 and claim 14 which is dependent therefrom are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

M. Claim 15

Claim 15 specifies that the on-chip registers include a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register. As described above, state of the art JTAG implementations put these registers in a separate chip. See Figure 1 of Texas Instruments.

Therefore claim 15 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

N. Claim 16

Claim 16 specifies that the size of the registers are each N-bits and that the microprocessor interface includes means for performing TAP operations having bit-counts in excess of N-bits. The Examiner refers to several pages in Texas Instruments which discuss registers, but it appears that the TAP operations described are limited to the size of the registers, i.e. 32-bits. Therefore claim 16 is patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

O. Claims 17 and 18

Claim 17 specifies that the means for performing TAP operations having bit-counts in excess of N-bits includes means for cycling the TAP through states. While Texas Instruments discusses TAP states required by the JTAG standard, there is no discussion of how to use these states to perform operations having bit counts in excess of the register size. Therefore claim 17 and claim 18 which depends therefrom are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness.

P. Claims 19 and 20

Independent claim 19 is drawn to an integrated circuit chip having core logic, an on-chip JTAG TAP, an on-chip JTAG master, an on-chip JTAG interface, and switching means for selectively coupling the JTAG master and the JTAG interface to the JTAG TAP. The Examiner's rejection of claim 19 is essentially the same as his rejection of claim 1 and the remarks made above regarding claim 1 apply to claim 19 as well. In addition, the only switching means shown in the prior art is the NTOE bit toggling which requires three chips and which does not couple the TAP to anything else when it is decoupled from the master. Therefore claim 19 and claim 20 which depends therefrom are patentable over the art of record because the Examiner has failed to make a prima facie case of obviousness and/or the applicant has otherwise overcome the Examiner's rejection.

In light of all of the above, it is submitted that the claims are in order for allowance, and the applicant respectfully requests that the Board direct the Examiner to allow the case.

Respectfully submitted,

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VIII. Claims Appendix

1. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG master coupled to said JTAG TAP; and

d) an on-chip microprocessor interface coupled to said JTAG master.

2. The chip according to claim 1, further comprising:

e) a plurality of registers coupled to said microprocessor interface and to said JTAG master.

3. The chip according to claim 2, wherein:

said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register.

4. The chip according to claim 3, wherein:

said plurality of registers includes a start bit register and an end bit register.

5. The chip according to claim 1, wherein:

said chip has more than five pins and five of said pins are coupled to said on-chip JTAG TAP forming a JTAG interface to said chip.

6. The chip according to claim 5, further comprising:

e) switching means for selectively decoupling said JTAG interface from said JTAG TAP.

7. The chip according to claim 6, wherein:

said switching means is coupled to and controllable by said JTAG master.

8. The chip according to claim 7, wherein:

said switching means couples said JTAG master to said JTAG TAP when said JTAG interface is decoupled from said JTAG TAP, and

said switching means couples said JTAG interface to said JTAG TAP when said JTAG master is decoupled from said JTAG TAP.

9. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG interface selectively coupled to said JTAG TAP;

d) an on-chip microprocessor interface selectively coupled to said JTAG TAP; and

e) switching means for selectively coupling said JTAG interface and said microprocessor interface to said JTAG TAP.

10. The chip according to claim 9, wherein:

said switching means operates to decouple said JTAG interface from said JTAG TAP when said microprocessor interface is coupled to said JTAG TAP, and

said switching means operates to decouple said microprocessor interface from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP.

11. The chip according to claim 9, wherein:

said microprocessor interface includes a plurality of registers.

12. The chip according to claim 9, wherein:

said switching means is controllable via said microprocessor interface.

13. The chip according to claim 12, further comprising:

f) a switching means enable interface for receiving a signal to enable said switching means, wherein

said switching means is inoperable without receiving said signal.

14. The chip according to claim 13, wherein:

in the absence of said signal said switching means decouples said microprocessor interface from said JTAG TAP and couples said JTAG interface to said JTAG TAP.

15. The chip according to claim 11, wherein:

said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register.

16. The chip according to claim 15, wherein:

said TDI FIFO and said TMS FIFO each being N-bits in size, and

said microprocessor interface includes means for performing TAP operations having bit counts in excess of N-bits.

17. The chip according to claim 16, wherein:

means for performing TAP operations having bit counts in excess of N-bits includes means for cycling said TAP through state elements and holding it in one of four states.

18. The chip according to claim 17, wherein:

said four states include Test-logic Reset, Run-Test Idle, Pause-IR, and Pause-DR.

19. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG master selectively coupled to said JTAG TAP;

d) an on-chip JTAG interface selectively coupled to said JTAG TAP; and

e) switching means for selectively coupling said JTAG master and said JTAG interface to said JTAG TAP.

20. The chip according to claim 19, wherein:

said switching means operates to decouple said JTAG interface from said JTAG TAP when said JTAG master is coupled to said JTAG TAP, and

said switching means operates to decouple said JTAG master from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.